IN THE CLAIMS:

Claims 1-30 (Cancelled)

Claim 31 (New) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells arranged in rows and columns, the memory cell array including a plurality of blocks in each one of which the memory cells are arranged; and

a word-line select circuit including transfer transistors arranged in row and column directions, and configured to select at least one row of memory cells from the plurality of memory cells in a block,

the word-line select circuit including,

first transistors to which OV is to be applied;

second transistors to which an intermediate level voltage is to be applied, the intermediate voltage being a voltage applied to a non-selected word line in a block selected in a writing operation; and

third transistors to which a write voltage is to be applied, the third transistors being separated from the first transistors.

Claim 32 (New) The semiconductor memory device according to claim 31, wherein first to third metal lines are provided to extend to the first to third word lines connected from the first to third transfer transistors to the memory cells, and are also located at a layer upper than a layer at which the first to third word lines are provided.

Claim 33 (New) The semiconductor memory device according to claim 31, wherein the memory cells each include a memory cell transistor having a floating gate that is electrically in a

floating state and a control gate stacked on the floating gate.

Claim 34 (New) The semiconductor memory device according to claim 31, wherein the memory cells each are NAND cells.

Claim 35 (New) The semiconductor memory device according to claim 34, wherein the NAND cells each include memory cell transistors, current paths of which are connected in series, and a select transistor connected to both or either one of an end of the memory cell transistors connected in series and an other end thereof.